

Fujitsu and Socionext Develop Next-Generation 56 Gbps Transceiver Circuit with World's Lowest Power Consumption for Optical Communications between Servers

Doubles communications speed at current power level, contributing to higher performance in next-generation servers

Kawasaki and Yokohama, Japan, February 1, 2016 --- Fujitsu Laboratories Ltd. and Socionext Inc. today announced that they have developed the world's lowest power-consuming transceiver circuit that achieves communications speeds of 56 Gbps per channel. Compared to previous levels, this essentially doubles the speed of data transfers between semiconductor chips, used in servers and switches, and optical modules.

There is an increasing need to accelerate data transfers between servers in response to improvements in the processing performance of datacenters; however, at the same time, limitations on the amount of electricity that facilities can supply mean that there is also a demand to lower electricity consumption.

Fujitsu Laboratories and Socionext have now developed a new timing detection method that combines the functions of the circuit that compensates signal degradation that becomes prominent as communication speeds improve with some of the functions of the timing-detection circuit that determines the bit-value of input signals, reducing the number of circuits. As a result, they succeeded in developing a 56 Gbps transceiver circuit that achieves twice the speed as before without raising power consumption.

This technology is able to increase the speed of data transfers between chips and optical modules without increasing power consumption, so it is expected to lead to performance improvements in next-generation servers and switches.

Details of this technology will be announced at the IEEE International Solid-State Circuits Conference 2016 (ISSCC 2016), the largest conference related to semiconductor technology, held from January 31 in San Francisco (ISSCC Presentation Number 3.5).

Development Background

In recent years, to support the rapidly expanding needs of cloud computing, there has been a demand for improvements in datacenter processing performance. Datacenters use numerous

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servers connected through switches to form a large-scale system, and as the processing ability of datacenters has improved, the volume of data exchanged between servers has also been further increasing.

For this reason, there has been progress in international standardization (*) of the communication speed of optical modules used for optical transmission between servers and switches for next-generation datacenters at 56 Gbps, twice current speeds.

At the same time, due to limitations on the amount of electricity that can be supplied in datacenters, there has been a demand for improvements in communication speed without increasing the amount of power consumed by data transceiver circuits.

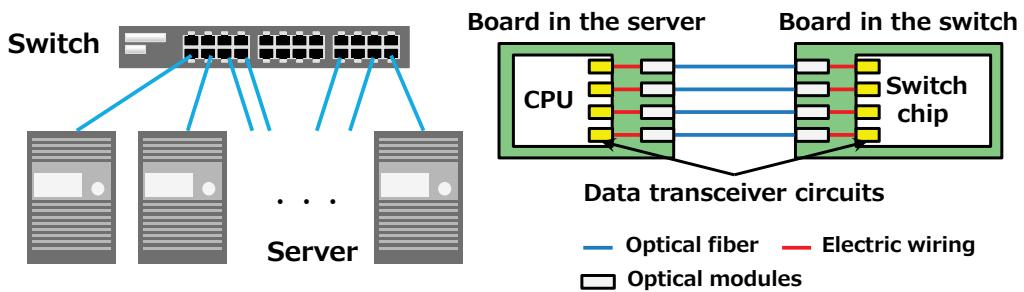


Figure 1: Transceiver circuits connecting servers and switches

Note (*) International standardization at 56 Gbps: Promoted by the Optical Internetworking Forum (OIF), an international standardization organization.

Issues

Power consumption increases proportionally with communication speed, making it necessary to decrease the power consumed by transceiver circuits in order to boost communication speed without increasing facility power.

In conventional transceiver circuits, the decision feedback equalizer (DFE), which is a circuit that compensates degraded signals, and the clock and data recovery (CDR) circuit, which detects timing errors between an incoming signal and the internal sampling clock, are responsible for about two thirds of the transceiver circuit's total power consumption, so reducing their power consumption has been a central issue.

For the input-signal waveform that became degraded in the transmission line, the bit value is determined at the determination circuits, one which has a $+a$ threshold value and the other a $-a$ threshold value. The DFE compensates the degraded signal by choosing the determination results of the $+a$ determination circuit if the previous bit value processed was a 1, or the results of $-a$ if the previous bit value processed was 0. The CDR, by observing the incoming signal, adjusts the DFE's operational timing to ensure it captures the signal when the incoming signal's waveform is at its greatest amplitude (Figure 2).

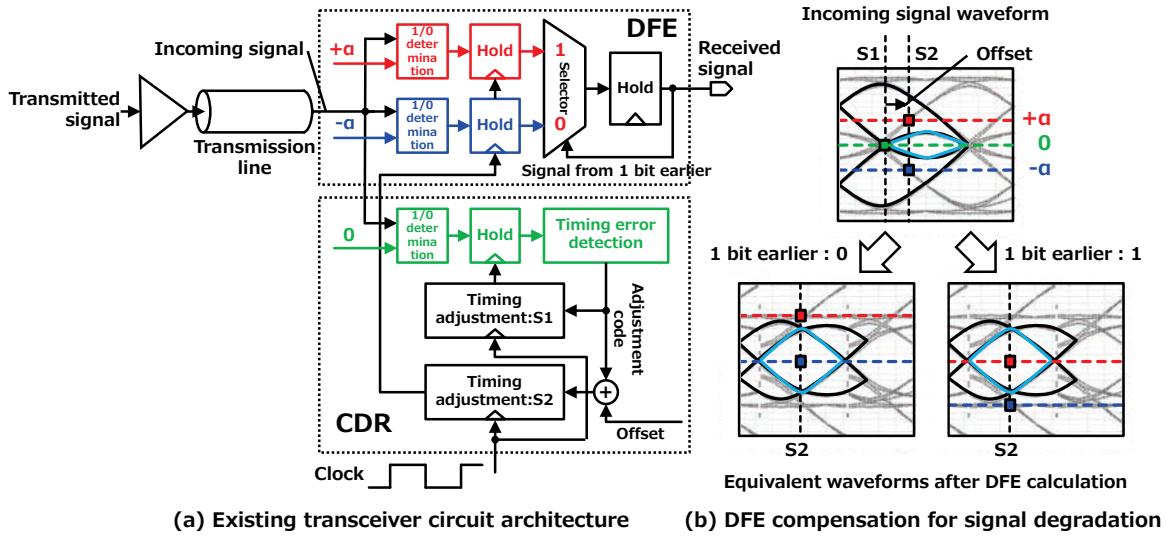


Figure 2: Existing transceiver circuit architecture and DFE compensation for signal degradation

Newly Developed Technology

To reduce the power consumption of the CDR, Fujitsu Laboratories and Socionext have now developed a new timing error detection method.

By analyzing waveforms after DFE calculation, Fujitsu Laboratories and Socionext discovered that they could detect whether the DFE's operational timing was early or late by comparing the results of the two DFE determination circuits in cases where three consecutive bits in the input signal were 100 or 011. This led them to develop a new timing detection method that only detects the timing when three consecutive bits of the incoming signal are 100 or 011 (Figure 3).

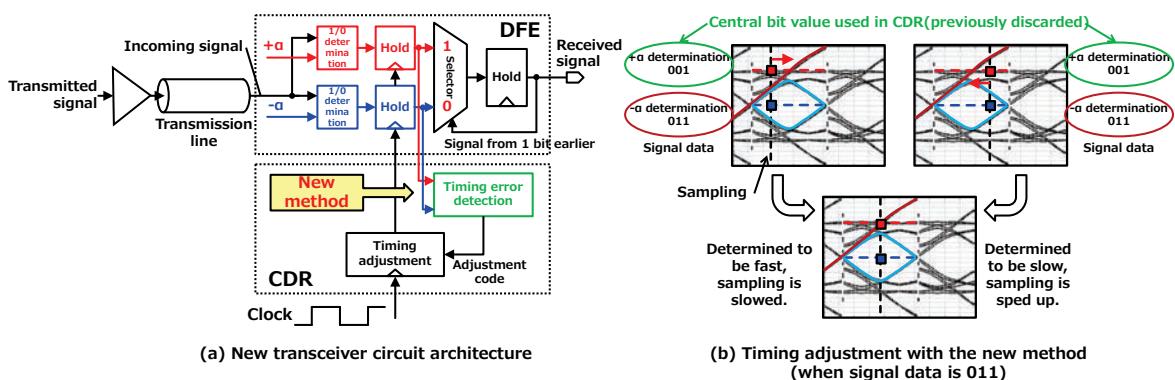


Figure 3: New transceiver circuit architecture and timing adjustment with the new method

With this newly developed timing detection method, the two companies were able to eliminate the previously required CDR incoming-signal timing-determination circuit, and lines, such as the clock line, which were required as the DFE and CDR operated with different timing. This made it possible for them to succeed in developing transceiver circuitry that doubles speeds to 56 Gbps with the same power consumption as before.

Effects

This new technology will be able to boost data transmission speeds between chips and optical modules without raising power consumption compared to the present. In addition, compatibility with upcoming OIF standards for optical module communications means that optical modules can be expected to be more compact and use less power, requiring half the number of transceiver circuits--from 16 to eight when using this technology--when constructing a 400 Gbps Ethernet with the current 28 Gbps standard.

Future Plans

Fujitsu Laboratories and Sionext will use the newly developed technology in interface components between optical modules and the chips of servers and switches, aiming for commercialization in fiscal 2018.

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About Fujitsu

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About Fujitsu Laboratories

Founded in 1968 as a wholly owned subsidiary of Fujitsu Limited, Fujitsu Laboratories Ltd. is one of the premier research centers in the world. With a global network of laboratories in Japan, China, the United States and Europe, the organization conducts a wide range of basic and applied research in the areas of Next-generation Services, Computer Servers, Networks, Electronic Devices and Advanced Materials. For more information, please see: <http://jp.fujitsu.com/labs/en>.

About Sionext Inc.

Sionext is a new, innovative enterprise that designs, develops and delivers System-on-Chip products to customers worldwide. The company is focused on imaging, networking and other dynamic technologies that drive today's leading-edge applications. Sionext combines world-class expertise, experience, and an extensive IP portfolio to provide exceptional solutions and ensure a better quality of experience for customers. Founded in 2015, Sionext Inc. is headquartered in Yokohama, and has offices in Japan, Asia, United States and Europe to lead its product development and sales activities. For more information, visit sionext.com.

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